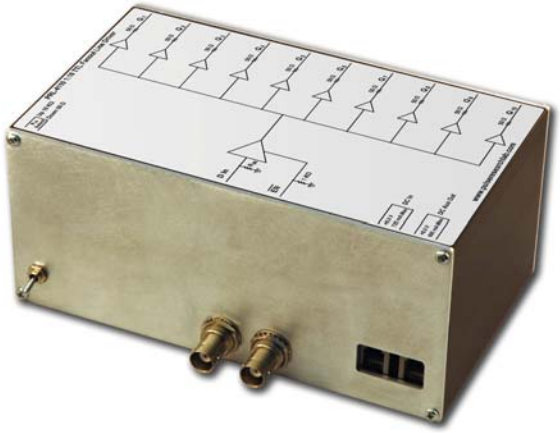
PRL-4110, 1:10 FANOUT 50 Ω TTL/CMOS LINE DRIVER

APPLICATIONS

- TTL/CMOS Clock Distribution
- 1:10 Fanout Line Driver
- High Speed Digital Communications System Testing
- Mini Modular Instrument

FEATURES

- f_{max} > 100 MHz
- Drives 100 ft of cable @ 80 MHz
- 1.8 ns Typical Output Rise & Fall Times
- 2.5 V into 50 Ω Typical
- TTL Compatible 50 Ω or 10 kΩ Input
- Ten in-phase 50 Ω TTL Outputs
- Active Low $\overline{EN}$ (Enable) Input
- BNC or SMA I/O Connectors
- DC Coupled I/Os
- Self-contained 3.0 x 6.8 x 4.0-in. unit includes an AC/DC Adapter



PRL-4110-BNC, Front View

PRL-4110-BNC, Rear View

DESCRIPTION:

The PRL-4110 is a 1:10 fanout, 50 Ω TTL Line Driver. It is intended for distribution of high-speed clock and logic signals to multiple loads via long lines. The 50 Ω back-terminated outputs can drive long lines with or without 50 Ω load terminations. With 50 Ω load terminations, however, all outputs of the PRL-4110 can drive 100 ft of 50 Ω cables at clock rates greater than 80 MHz.

The input resistance of the PRL-4110 can be selected to be either 50 Ω or 10 kΩ by a switch. The 10 kΩ-input is desirable when interfacing with low power circuits. The 50 Ω back terminated outputs typically deliver 2.5 V into 50 Ω or 5.0 V into Hi-Z loads. All I/Os are DC coupled and have BNC or SMA connectors (P/N PRL-4110-BNC or PRL-4110-SMA).

The unit also has a TTL-compatible $\overline{EN}$ input pulled down via a 1 kΩ resistor. When left open the Enable is active, and the fanout buffer will output signals. The unit can be disabled by driving its $\overline{EN}$ input high.

The PRL-4110 is housed in a 3.0 x 6.8 x 4.0-in. extruded aluminum enclosure and is supplied with the PRL-760B, ±8.5 V/±1.4 A AC/DC Adapter. The two DC power jacks are bussed together internally, allowing a second PRL-4110 to be daisy-chained from a single AC adapter. Two units can share a single PRL-760B adapter provided that the clock rate is 100 MHz or slower. The larger PRL-760C adapter, with point-to-point cabling, is recommended for multiple units at high data rates.

A block diagram showing the equivalent input and output circuits of the PRL-4110 is shown in Fig. 1.

RELATED PRODUCTS:

PRL-4220, 2:20 Fanout 50 Ω TTL Line Driver, equivalent to two PRL-4110 units in a single enclosure
PRL-4330, 3:30 Fanout 50 Ω TTL Line Driver, equivalent to three PRL-4110 units in a single enclosure
PRL-4122, 1:22 Fanout 50 Ω TTL Line Driver, equivalent to one PRL-414B driving two PRL-4110 units in a single enclosure

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SPECIFICATIONS* (0 ˚C ≤ T_A ≤ 35 ˚C)

Unless otherwise specified, dynamic measurements are made with the input set to 50 Ω and all outputs terminated into 50 Ω.

SYMBOL	PARAMETER	Min	Typ	Max	UNIT	Comments
$R_{IN\ Low}$	Input Resistance Low Range	49.5	50.0	50.5	Ω	
$R_{IN\ Hi}$	Input Resistance High Range	9.9	10.0	10.1	kΩ	
$R_{IN\ EN}$	Input Resistance, Enable		1		kΩ	
R_{OUT}	Output Resistance		50		Ω	
V_{IL}	TTL Input Low Level	-0.5	0.0	0.5	V	
V_{IH}	TTL Input High Level	2.0	2.4	5.0	V	
$V_{IL\ EN}$	$\overline{EN}$ Input Low Level	-0.5	0.0	0.5	V	
$V_{IH\ EN}$	$\overline{EN}$ Input High Level	2.0	2.4	5.0	V	Drive $\overline{EN}$ High to disable output
V_{OL}	TTL Output Low Level	0.0	0.25	0.5	V	R_L=50 Ω
V_{OH1}	TTL Output High Level	2.2	2.5		V	R_L=50 Ω @ DC
V_{OH2}	TTL Output High Level	4.4	5.0		V	R_L=1 MΩ @ DC
I_{DC1}	DC Input Current		500		mA	f =50 MHz sq. wave(1)
I_{DC2}	DC Input Current		615		mA	f ≤ 100 MHz
I_{DC3}	DC Input Current			725	mA	f =125 MHz
V_{DC}	DC Input Voltages	7.75	8.50	12.00	V	
V_{AC}	AC/DC Adapter Input Voltage	103	115	127	V	
T_{PLH}	Propagation Delay to output ↑		9	12	ns	
T_{PHL}	Propagation Delay to output ↓		9	12	ns	
t_r/t_f	Rise/Fall Times (10%-90%)		1.8/1.5	2.5	ns	
T_{SKEW}	Skew between any 2 outputs		500	900	ps	
F_{MAX1}	Max. Clock Frequency(2)	100	125		MHz	RG58C/U, cable length =3 ft
F_{MAX2}	Max. Clock Frequency		80			RG58C/U, cable length = 100 ft
PW_{MIN1}	Minimum Pulse Width		4		ns	↑ Input
PW_{MIN2}	Minimum Pulse Width		6		ns	↓ Input
	Size	3.0 x 6.8 x 4.0			in.	
	Weight	1.5			lb.	Excluding AC adapter

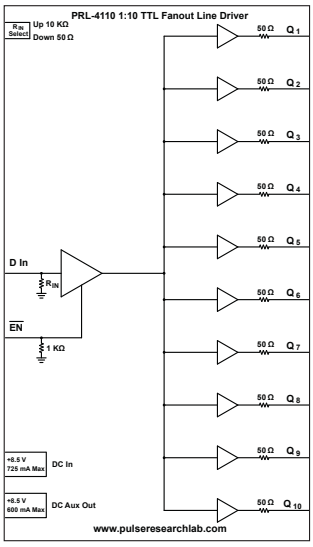

Fig. 1: PRL-4110 Block diagram

Notes:

(1) f_{MAX} should not exceed 125 MHz, otherwise damage of the unit due to overheating may result.

(2) f_{MAX2} is measured by driving a second PRL-4110 at the end of a 100 ft cable.

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