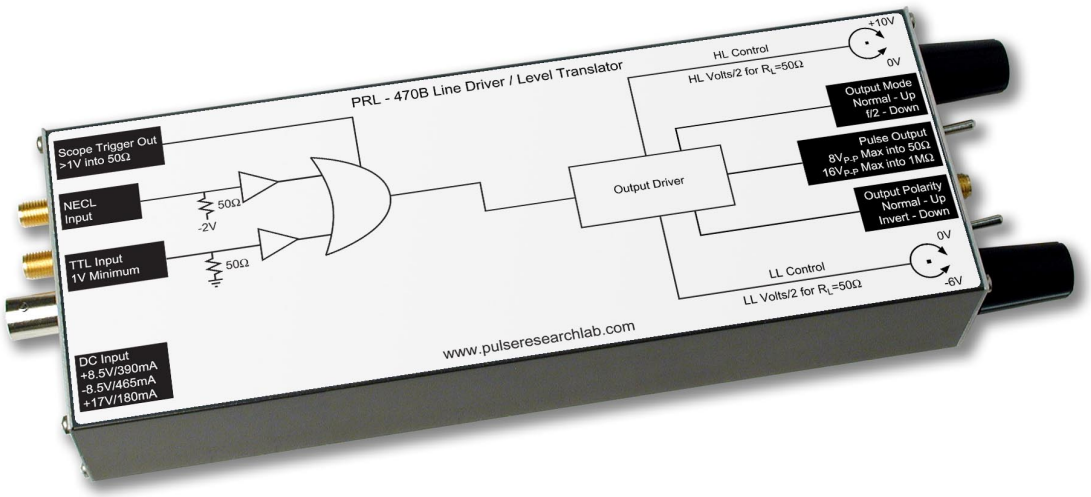
PRL-470B HIGH SPEED LINE DRIVER/LEVEL TRANSLATOR



Applications

- Long Line Driver/ Level Translator
- Laser Diode Driver
- TTL/CMOS/ECL Device Testing
- Amplifier Large Signal Response Testing
- TDR Source for Cable Testing
- A Basic Laboratory Tool (BLT)

Features

- t_r= 800 ps Typical @ 5 V Output into 50 Ω
- +5 V/-3 V Output HL/LL into 50 Ω
- Normal or Inverted Output
- f/2 Mode for Square Wave Output
- f_{max} to 300 MHz @ 3.5 V Output
- TTL and Single-ended NECL Compatible Inputs (logically ORed)
- Self-contained 1.3 x 2.9 x 8.1-in. Module includes an AC/DC adapter

GENERAL DESCRIPTION

The PRL-470B is a high speed 50 Ω Line Driver/Level Translator with independently variable output Hi and Lo levels. It has TTL and NECL-compatible inputs. The TTL input has a 50 Ω to ground termination, and the single-ended NECL input has a 50 Ω/-2 V termination. The TTL and NECL inputs are logically ORed; therefore a Hi level applied to either input can be used as a gate signal. The PRL-470B is an improved version of the earlier Model PRL-470A.

The output Hi and Lo levels are independently variable from 0 V to +5 V and 0 V to –3 V into 50 Ω, respectively, or +10 V and –6 V into 1 M Ω. The maximum output peak to peak swing is 8 V into 50 Ω, or 16 V into 1 MΩ. The back-terminated 50 Ω output can drive long 50 Ω lines with or without load termination. A Normal/Invert switch provides output logic polarity selection, and an f/2 switch provides square wave output. The 50 Ω TTL input requires less than 1 V for triggering.

The 800 ps rise time output makes the PRL-470B a cost effective TDR source for testing cables. Typical maximum clock rate is 300 MHz @3.5 V output and 250 MHz @5 V output, well suited for testing logic circuits of different families, amplifiers and many semiconductor devices.

The trigger output generates > 1 V into 50 Ω or > 2 V into high impedance, and is back-matched with 50 Ω for driving un-terminated loads. The self-contained 1.3 x 2.9 x 8.1-in module is supplied with a ±8.5 V/+17 V AC/DC adapter.

Multiple PRL-470B modules together with other PRL logic function modules, such as Clock Sources, Fanout devices, Frequency Dividers, Programmable Delay Lines, Logic Level Translators, etc., can be rack-mounted for systems test applications. Consult factory for more information.

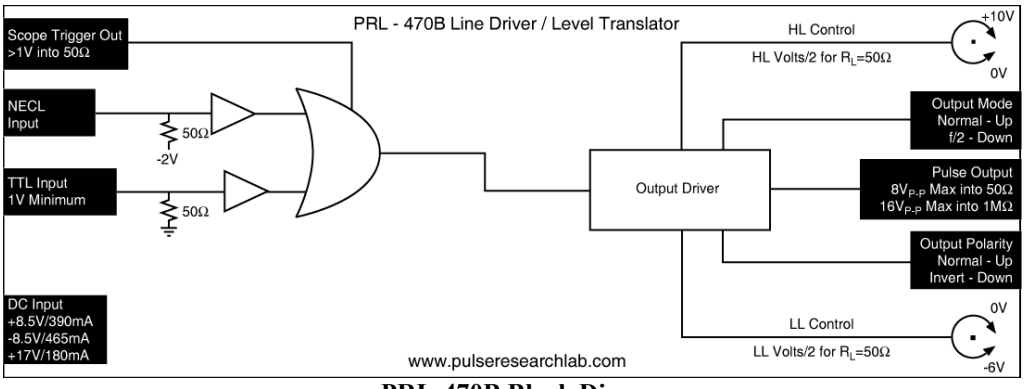
PULSE RESEARCH·LAB

1234 Francisco Street, Torrance, CA 90502
Tel: 310-515-5330 Fax: 310-515-0068
Email: sales@pulseresearchlab.com
www.pulseresearchlab.com

SPECIFICATIONS (0^0 C ≤ T_A ≤ 35^0C)

Unless otherwise specified, dynamic measurements are made with all outputs terminated into 50Ω.

SYMBOL	PARAMETER	Min	Typ	Max	UNIT	Comments
R_{in}	Input Resistance	49.5	50	50.5	Ω	
R_{in}/V_{TT}	TTL Input Termination NECL Input Termination		50 Ω to ground 50 Ω/-2 V			
V_{IL}	TTL input Low Level NECL input Low Level	-0.5 -2.4	0 -1.8	0.5 -1.5	V	
V_{IH}	TTL input High Level NECL Input High Level	0.8 -1.0	0.85 -0.8	5.0 -0.5	V	
V_{OL}	Output Low Level	-3/-6		0	V	R_L=50 Ω/1 MΩ
V_{OH}	Output High Level	0		5/10	V	R_L=50 Ω/1 MΩ
Vp-p	Output Voltage Swing	0.8/1.6		8/16	V	R_L=50 Ω/1 MΩ
I_{DC}	Max. DC Input Currents		+380/-450 +140	+390/-465 +180	mA	+8.5 V/-8.5 V +17 V
V_{DC}	DC Input Voltages	±8.5 +15	±9.5 +17.5	±12 +20	V	From PRL-760B AC adaptor @ 120VAC
V_{AC}	AC/DC Adapter Input Voltage	108	120	132	V	
t_{PLH}/t_{PHL} Vo	Prop. Delay to Output ↑/↓		5.5	7.5	ns	V_{OL}=0 V, V_{OH}=5 V
t_{PLH}/t_{PHL} Vot	Prop. Delay to Trigger Output ↑/↓		2.5	3.5	ns	
t_{r1}/t_{f1}	Output Rise/Fall Times (10%-90%)		0.8/1.4	0.9/1.65	ns	V_{OL}=0 V, V_{OH}=5 V
t_{r2}/t_{f2}	Output Rise/Fall Times (10%-90%)		0.75/1.2	0.8/1.3	ns	V_{OL}=0 V, V_{OH}=3.5 V
t_{r3}/t_{f3}	Output Rise/Fall Times (10%-90%)		0.75/1.2	0.8/1.2	ns	V_{OL}=-2.5 V, V_{OH}=2.5 V
t_{r4}/t_{f4}	Output Rise/Fall Times (10%-90%)		0.9/1.6	1.1//2	ns	V_{OL}=-3 V, V_{OH}=5 V
T_{SKEW}	Skew between Vo↑ and Vo↓		100	300**	ps	V_{OL}=0 V, V_{OH}=5 V F=50 MHz, PW=5 ns
Fmax1	Maximum Clock Frequency	225	250		MHz	V_{OL}=0 V, V_{OH}=5 V
Fmax2	Maximum Clock Frequency	250	300		MHz	V_{OL}=0 V, V_{OH}=3.5 V
Fmax3	Maximum Clock Frequency	250	300		MHz	V_{OL}=-2.5 V, V_{OH}=2.5 V
Fmax4	Max. Input Clock Frequency	500	600		MHz	Square Wave Mode
PW_{Min}	Minimum Output Pulse Width		2	2.5	ns	Vp-p=5 V
ΔPW	Output PW change, Vo↑ to Vo↓		200	400*	ps	Vo=0 to 5 V, PW=5 ns
Vo Trig	Trigger Output	1	1.2		V	R_L=50 Ω, f ≤ 250 MHz
	Size		1.3 x 2.9 x 8.1		in.	
	Weight		13		Oz	



PRL-470B Block Diagram

* Skew and ΔPW may vary with different output level, frequency and pulse width settings

PULSE RESEARCH LAB

1234 Francisco Street, Torrance, CA 90502
Tel: 310-515-5330 Fax: 310-515-0068
Email: sales@pulseresearchlab.com
www.pulseresearchlab.com